Amendments to the Specification:

Please insert the following new paragraphs in the SUMMARY OF THE INVENTION section on page 6, between lines 12 and 13:

One aspect provides a semiconductor integrated circuit for processing a plurality of received broadcast signals, the broadcast signals being of a type each having a different respective known digital code. The semiconductor integrated circuit includes:

a digital sampler;

a sample reducer; and

a plurality of correlators being arranged to be operable in two modes wherein:

in an acquisition mode:

the digital sampler samples the received broadcast signals to produce a digital bit stream at a first bit rate;

the sample reducer reduces bits of the digital bit stream by combining groups of N bits together to produce a reduced digital bit stream;

the plurality of correlators receive the reduced digital bit stream at a second bit rate, being higher than the first bit rate, and each of the plurality of correlators correlates the reduced digital bit stream with a same locally generated version of one of the different known digital codes; and

in a tracking mode:

the digital sampler samples the received broadcast signals to produce a digital bit stream at the first bit rate and provides that digital bit stream direct to each of the plurality of correlators, each correlator correlates that digital bit stream with a different locally generated version of one of the known digital codes.

According to one aspect, in acquisition mode, the second bit rate is a factor M higher than the first bit rate.

According to one aspect, there are Y correlators such that in acquisition mode a correlation rate is a factor X = N (bits) x M (bit rate factor) x Y (correlators) faster than a correlation rate in tracking mode for one of the known digital codes.

According to one aspect, the factor X is chosen to be substantially equal or greater than twice a number of bits in the known code, wherein all possible correlations of the code are performed before the code repeats.

Another aspect provides a method of processing a plurality of received broadcast signals each having a different respective known digital code. The method includes:

sampling the received broadcast signals to produce a digital bit stream at a first bit rate;

reducing bits of the digital bit stream by combining groups of N bits to produce a reduced bit stream;

correlating the reduced digital bit stream at a second bit rate using a plurality of correlators each correlating the reduced digital bit stream with a same one of a locally generated version of the known digital codes to acquire the broadcast signals; and

subsequently correlating the digital bit stream at the first bit rate using the plurality of correlators each correlating the reduced digital bit stream with a locally generated version of a different one of the known digital codes to track the previously acquired signals.

According to one aspect, the second bit rate is a factor M higher than the first bit rate.

According to one aspect, there are Y correlators such that when correlating to acquire, a correlation rate is a factor X = N (bits) x M (bit rate factor) x Y (correlators) faster than a correlation rate when tracking the acquired signals.

According to one aspect, the factor X is chosen to be substantially equal or greater than twice a number of bits in the known code, wherein all possible correlations of the code are performed before the code repeats.

Please replace the paragraph beginning on page 9, line 21 and ending on page 10, line 2 with the following redlined paragraph:

One embodiment of the decimator 26 is shown in Figure 4 and comprises a shift register 60 and adder 62. The decimator sums N samples together (here 8 samples are summed) to produce an output on line 63. In this example, 8 samples of the digitized received signal are summed giving possible outputs -8 to +8. To represent the possible outputs, the output values 0, 1, 2 or 3 are represented as logic "0" and outputs 5, 6, 7 or 8 are represented as logic "1". To prevent any bias in the output, the value 4 is represented as alternately logic "0" and logic "1". The output on line 63 is therefore a digital bit sequence which is a downsampled version of the digitized received signal without any information being discarded.

Please replace the paragraph beginning on page 11, lines 16-29 with the following redlined paragraph:

An incoming signal is mixed down by gate 44, fed with a locally generated 4.092 MHz. A decimator 26 comprises combinatorial logic to combine groups of 8 samples to reduce the sample rate without discarding information as before. It is noted, for the avoidance of doubt, that the decimation is not simply removing every 10^{th} sample. The decimated signal is loaded to a shift register 28 having multiple taps 29 which feed to correlators 30. The shift register is operable, when loaded, to circulate at a higher speed than the loading speed, such as 66 MHz or 200 MHz, preferably 128 MHz in one example embodiment. Each tap 29 feeds a separate correlator 30 (only one being shown for simplicity). A code generator 36 generates a local version of the respective CA code and applies this to the correlator 30. The correlator includes combinatorial logic (e.g., multiplexer 32) which combines the local version of the CA code with the decimated received signal from the tap points 29 of the circulating shift register. A low pass filter 34 provides the output.